AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 5, line 17, and ending on page 6, line 5, with the following amended paragraph:

However, in recent system LSIs, a microcomputer installed therein has been made to operate [[in]] at higher speed, and thus the instruction execution frequency per predetermined time is also made higher, whereby it is made more difficult that the microcomputer extracts trace information from a limited number of connection terminals. Fig. 15 is a block diagram showing the inner construction of the trace control circuit 115 shown in Fig. 14, focussing on the circuit portion related to a generation of branch events. In the trace control circuit of this example, the length of address data is 16 bits, and the length of data to be processed is also 16 bits. In Fig. 15, numeral 131 denotes a branch event generation circuit, 132 denotes a CPU-access event generation circuit, 133 denotes a selector, 134 denotes a trace memory, 135 denotes a trace data output circuit, 136 denotes an OR gate, 137 denotes a status information generation circuit, 138 denotes an address data latch circuit for latching 16-bit data, 139 denotes an AND gate, 140 denotes an address data latch circuit for latching 16-bit data, 141 denotes an ~~ADN~~ AND gate, 142 denotes a buffer, and 143 denotes an AND gate.

Please replace the paragraph beginning on page 10, line 8, with the following amended paragraph:

The present invention has been proposed to solve the problems aforementioned, and it is an object of the present invention to provide a trace control circuit capable of tracing the operation of a CPU ~~rather~~ in real time.

Please replace the paragraph beginning on page 19, line 20, and ending on page 20, line 20, with the following amended paragraph:

Thereafter, when the write signal TYRW1 provided as an ANDed signal of the selection signal SEL1 and the base clock signal P1 from the AND gate 22 becomes H level, 40-bit data composed of the status information, the branch-destination address abbreviation information, the branch-source address data and the branch-destination address data is ~~write~~ written into the trace memory 4. Thereafter, when the synchronous signal SYNC for tracing becomes H level, the trace data circuit 5 reads out the data from the trace memory 4, and sequentially outputs trace data from the data signal terminal "DATA" in synchronism with the clock signal CLK for tracing per 4 bits at each time. On this occasion, the trace data abbreviation circuit 5 abbreviates overlapped bit strings of the branch-source address with those of the branch-destination address sequentially from the upper address sides thereof, and outputs the partly abbreviated trace data. Various data are output from the data signal terminal "DATA" in the order of the status information ST1 that indicates the type of the trace event, the branch-destination address abbreviation information ST2, branch-source address (ASLL, ASLH, ASHL, ASHH), and the branch-destination address (ADLL, ADLH, ADHL, ADHH), some part of which has been abbreviated. On this occasion, due to the fact that the branch-destination address abbreviation information ST2 indicates that the upper 8-bit portion of the branch-destination address coincides with that of the branch-source address, the trace data with [[the]] this upper 8-bit portion of the branch-destination address ~~been~~ being abbreviated is output. For this reason, by employing the above circuit configuration, although 9

clock signal cycles for tracing (hereinafter may be referred to as "CLK cycle" or just as "CLK") have been required conventionally for outputting the trace data related to the branch event, the minimum required cycle can be reduced to only 6 cycles (8 cycles in the above case).